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UTILITY APPLICATION FOR UNITED STATES PATENT
FOR
MICROWAVE POWER AMPLIFIER

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MICROWAVE POWER AMPLIFIER

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a microwave power amplifier, in particular, to the microwave power amplifier using negative feedback circuits, RC parallel circuits, and shunt resistors.

DESCRIPTION OF THE PRIOR ART

High-valued gains in a low frequency band are obtained due to a device's characteristic when designing a power amplifier in the millimeter-wave band. And, an oscillation may always occur in the low frequency band due to a limitation of modeling.

In the prior art, a feedback circuit has been employed in the power amplifier for stabilizing the amplifying device. For example, see the following publication that is incorporated herein by reference: IEEE Trans. On MTT, Vol 49 to Joao Caldinhas Vaz et al entitled "Millimeter-Wave Monolithic Power Amplifier for Mobile Broad-Band Systems" issued in June 2001, which discloses a MMIC (microwave monolithic integrated circuit) power amplifier for applying to a 60GHz MBS (Mobile Broad-Band System). In this publication the 3-stage MMIC power amplifier was designed in two types such as a single-ended type and a balanced type by using 0.15um PMHFET (Peudomorphic heterojunction FET), and applies a RC feedback

1 network to first and second stage transistors in negative feedback manner for
2 achieving unconditional stability of a millimeter-wave transistor.

3 In addition, Korea patent number 2000-81018 that is incorporated
4 herein by reference and issued on December 23, 2000, discloses a radio
5 frequency power amplifier using a feedback circuit and a method for
6 designing the amplifier, wherein a feedback circuit is inserted in each stage of
7 the power amplifier so that an unstable amplifying element is absolutely
8 stabilized. It is designed by finding a peak output power point due to an
9 output power change according to an input power of a whole power amplifier
10 circuit, after stabilizing an unstable amplifier device using the feedback circuit
11 in a radio frequency band.

12 Hereinafter, the feedback microwave power amplifier in accordance
13 with the prior art will be explained with reference to Fig. 1 and 3.

14 Fig. 1 shows a circuit for explaining a feedback microwave power
15 amplifier in accordance with the prior art, which consists of gate bias circuit
16 101, 103, 105, drain bias circuit 102, 104, 106, negative feedback circuit 107,
17 109, HEMT (High Electron Mobility Transistor) devices 113, 114, 115, 116,
18 inter-stage matching circuits 108, 110, a power divider 111, and a power
19 combiner 112.

20 Referring to Fig. 1, a 3-stage power amplifier utilizes feedback
21 circuits 107, 109 in the first stage and the second stage to meet stability
22 conditions, and interstage matching circuits 108, 110 are connected between
23 stages to obtain interstage matching. Gate bias circuits 101, 103, 105 and
24 drain bias circuits 102, 104, 106 are separately applied to each stage, and at

1 the last stage, HEMT devices 115, 116 are connected in parallel with each
2 other by applying the power divider 111 and the power combiner 112 to
3 enhance power characteristics.

4 Fig. 3 shows a graph representing input/output characteristics and gain
5 of the feedback microwave power amplifier shown in Fig. 1.

6 Referring to Fig. 3, when the power amplifier was designed by using
7 only a feedback circuit, unconditional stability conditions were met in terms of
8 stability. However, when only a negative feedback circuit is applied to the
9 power amplifier, potential oscillation may occur at any time due to a mis-
10 match in a low frequency band, as is shown in gain characteristics 301 and
11 input return loss characteristics 302 in the low frequency band. In other
12 words, the power amplifier employing the feedback circuit in accordance with
13 the above described prior art still has a potential oscillation problem in the low
14 frequency band.

16 SUMMARY OF THE INVENTION

17 Therefore, the object of the present invention is to provide a single
18 chip microwave power amplifier capable of being stable from the low
19 frequency band to the microwave band by using negative feedback circuits,
20 RC parallel circuits, and shunt resistances.

21 To achieve the above object, the microwave power amplifier
22 comprises a drive amplifying stage including power devices, gate and drain
23 bias circuits of said power devices, a RC parallel circuit connected between
24 input port and gates of said power devices, a shunt resistor connected between

1 ground terminal and said gates of power devices, and a negative feedback
2 circuit connected in series with resistors and capacitors and in parallel with
3 said power devices; an interstage matching circuit connected in series with
4 said drive amplifying stage; and a power amplifying stage including power
5 devices connected in parallel with a power divider and a power combiner, gate
6 and drain bias circuits of said power devices, a RC parallel circuit connected
7 between said gates of power devices and said interstage matching circuit, and
8 a shunt resistor connected between a ground and said gates of power devices.

9

10 **BRIEF DESCRIPTION OF THE DRAWINGS**

11 Fig. 1 shows a circuit for explaining a feedback microwave power
12 amplifier in accordance with the prior art.

13 Fig. 2 shows a circuit for explaining a configuration of the microwave
14 power amplifier in accordance with a preferred embodiment of the present
15 invention.

16 Fig. 3 shows a graph representing input/output characteristics and gain
17 of the feedback microwave power amplifier shown in Fig. 1.

18 Fig. 4 shows a graph representing input/output characteristics and gain
19 of the feedback microwave power amplifier shown in Fig. 2.

20 Fig. 5 shows a layout of Fig. 2.

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22 **DESCRIPTION OF THE PREFERRED EMBODIMENTS**

23 Hereinafter, embodiments of the present invention will be explained
24 with reference to the accompanying drawings. Although the present invention

1 has been described in conjunction with the preferred embodiment, the present
2 invention is not limited to the embodiments, and it will be apparent to those
3 skilled in the art that the present invention can be modified in variation within
4 the scope of the invention.

5 Fig. 2 shows a circuit for explaining a configuration of the microwave
6 power amplifier in accordance with a preferred embodiment of the present
7 invention. The circuit includes a first drive amplifying stage 200, a second
8 drive amplifying stage 240, and a third power amplifying stage 280.
9 Hereinafter, the microwave power amplifier using a negative feedback circuit,
10 a RC parallel circuit, and a shunt resistor in accordance with the preferred
11 embodiment of the present invention will be described in detail.

12 Referring to Fig. 2, the microwave power amplifier using negative
13 feedback circuits, RC parallel circuits, and shunt resistances uses negative
14 feedback circuits 207, 209, RC parallel circuits 217, 219, and shunt resistors
15 218, 220 in drive stages such as the first drive amplifying stage 200 and the
16 second drive amplifying stage 240 in order to meet unconditional stability
17 conditions and broadband characteristics. In addition, a RC parallel circuit
18 221 and a shunt resistor 222 are utilized in a power stage such as the third
19 power amplifying stage 224 to meet absolute stability conditions. The power
20 matching is achieved to obtain maximum output power by using the power
21 divider 211 and the power combiner 212, with amplifying devices 215, 216
22 formed in parallel with each other. The inter-stage matching circuits 208, 210
23 may be inserted between the first drive amplifying stage 200 and the second
24 drive amplifying stage 240, and between the second drive amplifying stage

1 240 and the third power amplifying stage 280. The inter-stage matching
2 circuits 208, 210 may include micro-strip lines and open stubs. The inter-
3 stage matching circuits 208, 210 function as supplying gain without loss with
4 regard to power matching of the output. Those inter-stage matching circuits
5 208, 210 may be separated by capacitors for DC blocking between each of
6 stages.

7 The first drive amplifying stage 200 includes a power device 213 for
8 raising signal level, input matching circuits 201, 217, 218 designed for
9 transmitting input signal without loss, a RC parallel circuit 217, a shunt
10 resistor 218, a negative feedback circuit 207, a gate bias circuit 201, and a
11 drain bias circuit 202.

12 The power device 213 can be implemented as a HEMT (High Electron
13 Mobility Transistor), and the RC parallel circuit 217 is connected in series
14 between the input port and the gate of the power device 213, and the shunt
15 resistor 218 is connected between the ground terminal and the gate stage of the
16 power device 213. The shunt resistor 218 is a resistor having micro-strip lines
17 connected to both ends thereof, and the ground terminal can be formed of via-
18 holes. A matching component with the input stage can be adjusted by
19 changing resistance of the shunt resistor and adjusting a length of the micro-
20 strip line. And, the negative feedback circuit 207 including resistors and
21 capacitors is positioned in parallel with the power device 213, thereby making
22 an amplifying portion. The gate bias circuit 201 and the drain bias circuit 202
23 are separated for supplying independent biases, respectively, and it is
24 preferable to provide the DC supply with a pad of GPPPPGPPG (Ground-Pad-

1 Pad-Pad-Pad-Ground-Pad-Pad-Ground) type having 200um pitch for on-wafer
2 measurement. The interstage matching circuit 208 is connected to the output
3 portion of the power device 213.

4 The second drive amplifying stage 240 is connected to the first drive
5 amplifying stage 220 through the interstage matching circuit 208 and has the
6 same configuration as the first drive amplifying stage 200. In other words, the
7 second drive amplifying stage 240 includes the power device 214 for
8 increasing signal level, the RC parallel circuit 219, the shunt resistor 220, the
9 negative feedback circuit 209, the gate bias circuit 203, and the drain bias
10 circuit 204.

11 The power device 214 of the second drive amplifying stage 240 can
12 also be implemented as the HEMT (High Electron Mobility Transistor), and
13 the RC parallel circuit 219 is connected in series between the interstage
14 matching circuit 208 and the gate of the power device 214, and the shunt
15 resistor 220 is connected between the ground terminal and the gate stage of the
16 power device 214. The shunt resistor 220 is a resistor having micro-strip lines
17 connected to both ends thereof, and the ground terminal can be formed of via-
18 holes. And, the negative feedback circuit 209 includes resistors and capacitors
19 positioned with the power device 214 in parallel, and the interstage matching
20 circuit 210 is displaced in the output portion of the power device 214. The
21 gate bias circuit 203 and the drain bias circuit 204 are separated for supplying
22 independent biases, respectively, and it is preferable to provide the DC supply
23 with a pad of GPPPPGPPG (Ground-Pad-Pad-Pad-Pad-Ground-Pad-Pad-
24 Ground) type having 200um pitch for on-wafer measurement.

1 The third power amplifying stage 280 includes power devices 215,
2 216 for amplifying signals transmitted from the first drive amplifying stage
3 200 and the second drive amplifying stage 240, a RC parallel circuit 221, a
4 shunt resistor 222, a gate bias circuit 205, a drain bias circuit 206, a power
5 divider 211, and a power combiner 212. The third power amplifying stage 280
6 is connected to the second power amplifying stage 240 through the inter-stage
7 matching circuit 210. It is designed to distribute input signals without loss
8 using the power divider 211 and the power combiner 212, amplify input
9 signals by means of power devices 215, 216 connected in parallel and output
10 the amplified signals coupled without loss, while unconditional stability is
11 maintained using the RC parallel circuit 221 and the shunt resistor 222.

12 Fig. 4 shows a graph representing input/output characteristics and gain
13 of the feedback microwave power amplifier shown in Fig. 2. In terms of gain
14 and input/output characteristics, a result of design shown in Fig. 2, it can be
15 seen that unconditional stability in whole band from the low frequency band to
16 the microwave band, while the possibility of oscillation due to a mis-match is
17 completely eliminated, as is shown in the input return loss characteristic 402
18 and gain characteristic 401 in the low frequency band.

19 Fig. 5 shows a layout of Fig. 2. As shown in Fig. 5, the power
20 amplifier of the present invention is designed such that the RC parallel circuit
21 is positioned in series between the gate of the power device and the input port
22 of the first drive amplifying stage, a resistor between the ground terminal and
23 the gate, and the negative feedback circuit includes resistors and capacitors is
24 connected in parallel with power devices. The second drive amplifying stage

1 is connected to the first drive amplifying stage through the interstage matching
2 circuit. And, the third power amplifying stage is connected to the second
3 drive amplifying stage through the interstage matching circuit.. Thus, the
4 power amplifier is implemented as one chip such as integrated circuit.

5 As described above, the microwave power utilizes negative feedback
6 circuits, RC parallel circuits, and shunt resistors, and has advantages in that it
7 can be designed to control undesired input return loss characteristic and gain
8 characteristic in the low frequency band, and completely block oscillation in
9 the low frequency band, compared to the conventional power amplifier only
10 using feedback circuits.

11 Therefore, it can have unconditional stability characteristic from the
12 low frequency band to the microwave band, and input matching can be
13 facilitated so that it is applicable in design of a microwave integrated circuit
14 amplifier in the millimeter band.

15 Although the present invention has been described in conjunction with
16 the preferred embodiment, it is not limited to the embodiments, and it will be
17 apparent to those skilled in the art that the present invention can be modified
18 in variation within the scope of the invention.